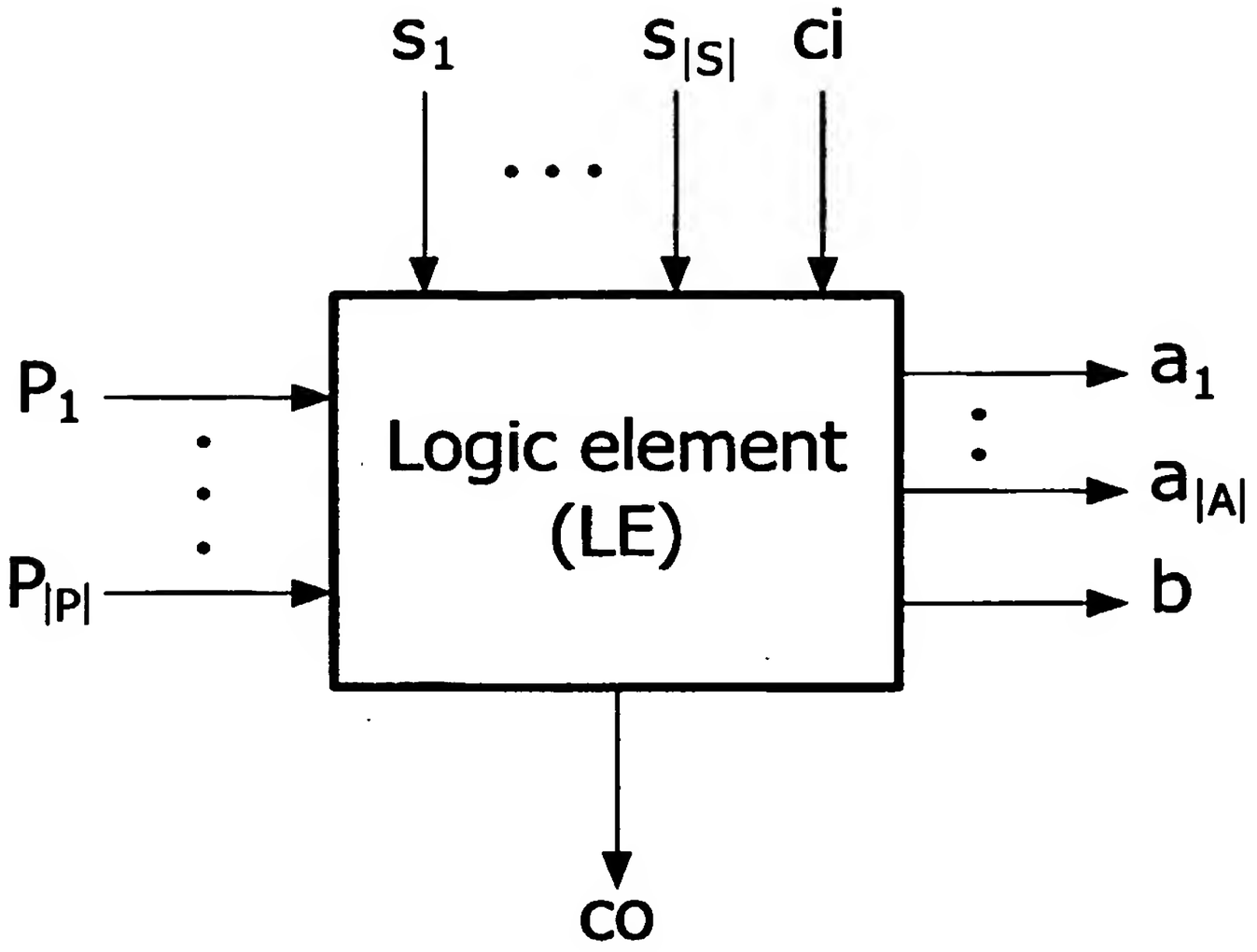

FIG. 1

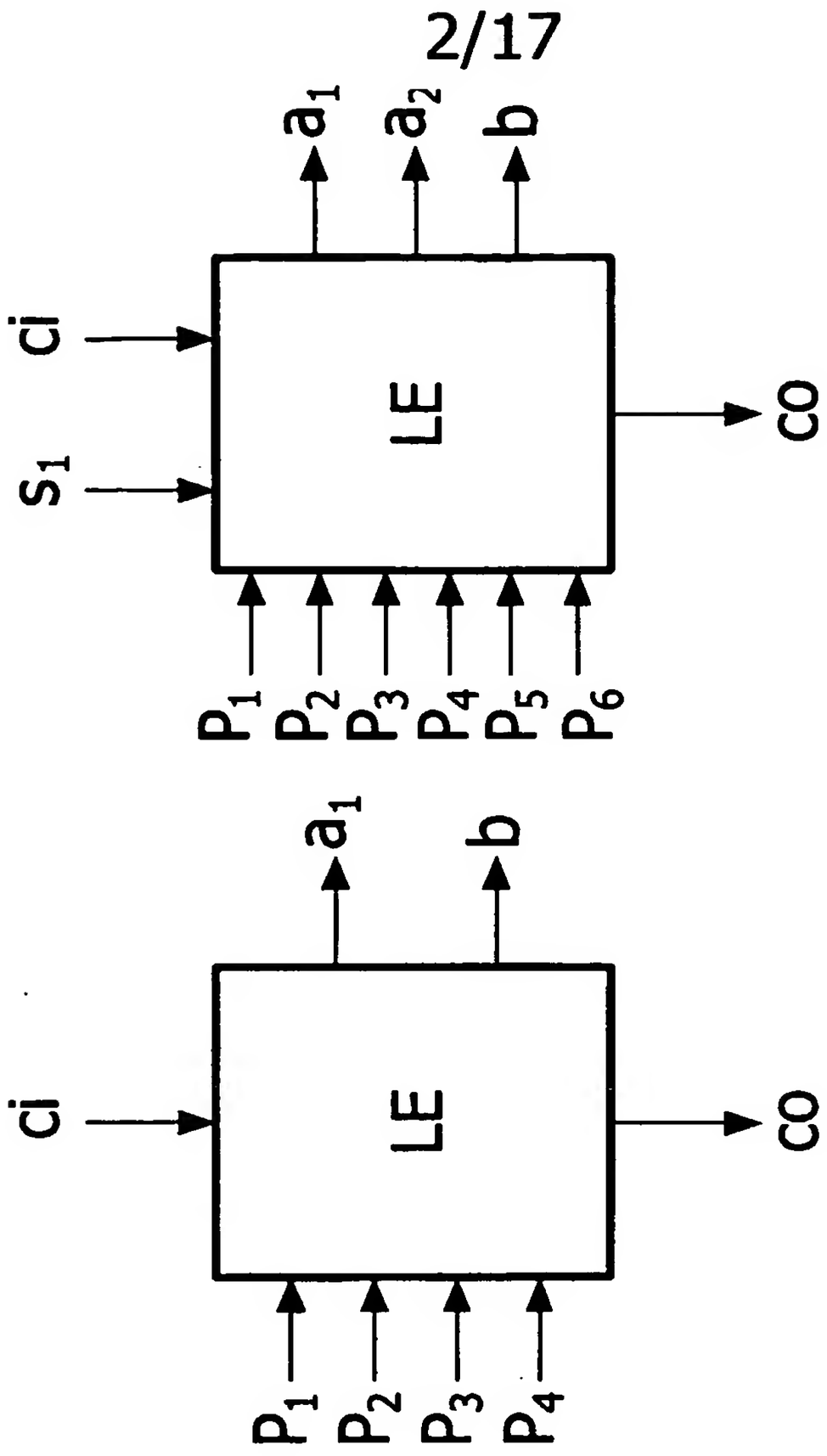

FIG. 2c

FIG. 2b

FIG. 2a

TYPE	|P|	|S|	|A|
Data-path oriented	2	3	1
Random-logic oriented	4	0	1
Memory-oriented	6	1	2

FIG. 3

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	2	1	-
Random-logic oriented	4	1	-
Memory-oriented	5	2	2

FIG. 4

TYPE	|X|	|S|	|Y|
Data-path oriented	2*|N|	3	|N|
Random-logic oriented	max(log|N| + 4,2*|N|)	0	|N|
Memory-oriented	6*|N|	1	2*|N|

FIG. 6

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	log|N| + 2	|N|	-
Random-logic oriented	log|N| + 4	|N|	-
Memory-oriented	log|N| + 5	2*|N|	2*|N|

FIG. 7

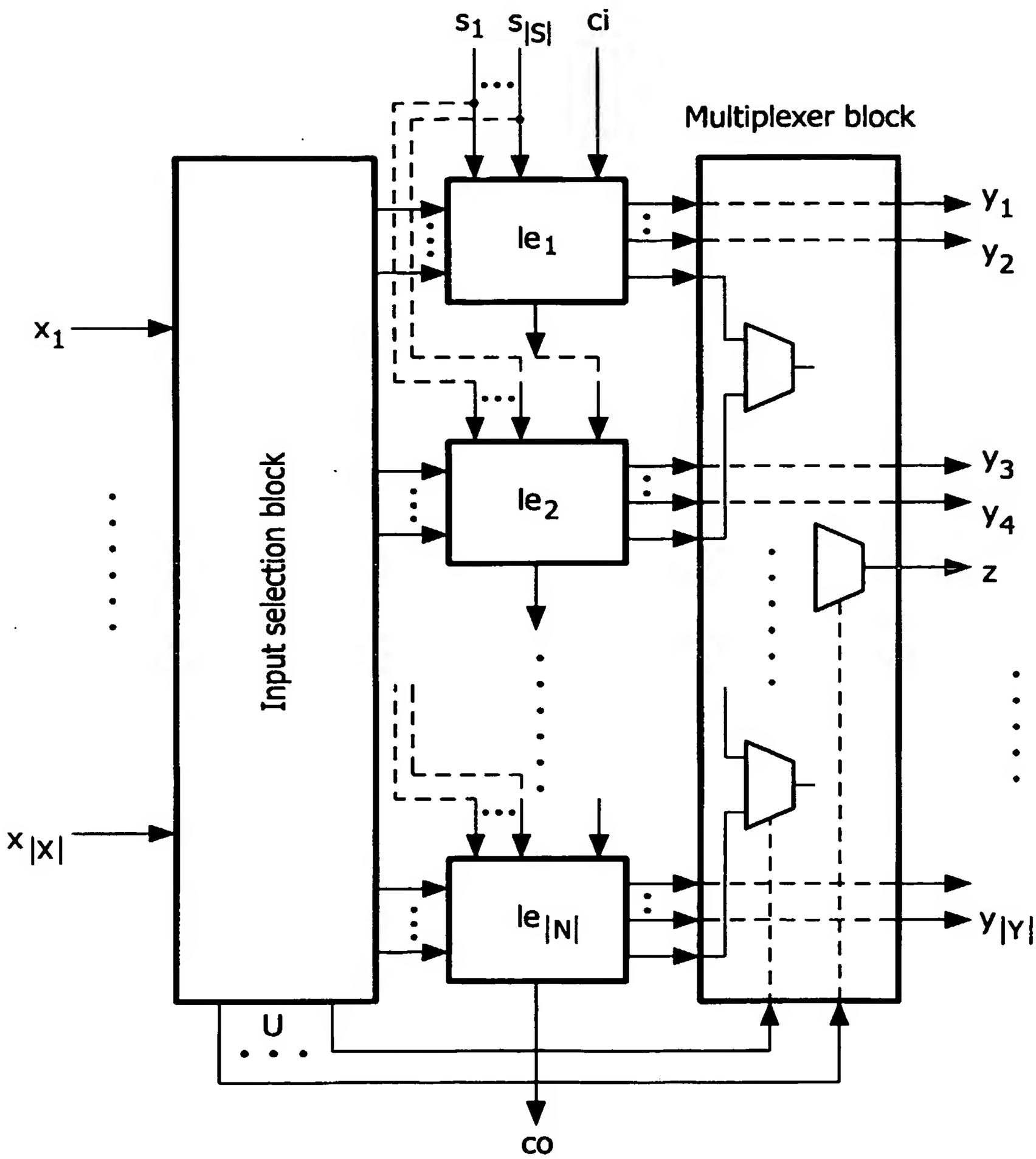
s1
s|S|
ci
Multiplexer block
le1
le2
le|N|
x1
x|X|
Input selection block
y1
y2
y3
y4
z
y|Y|
U
co

FIG. 5

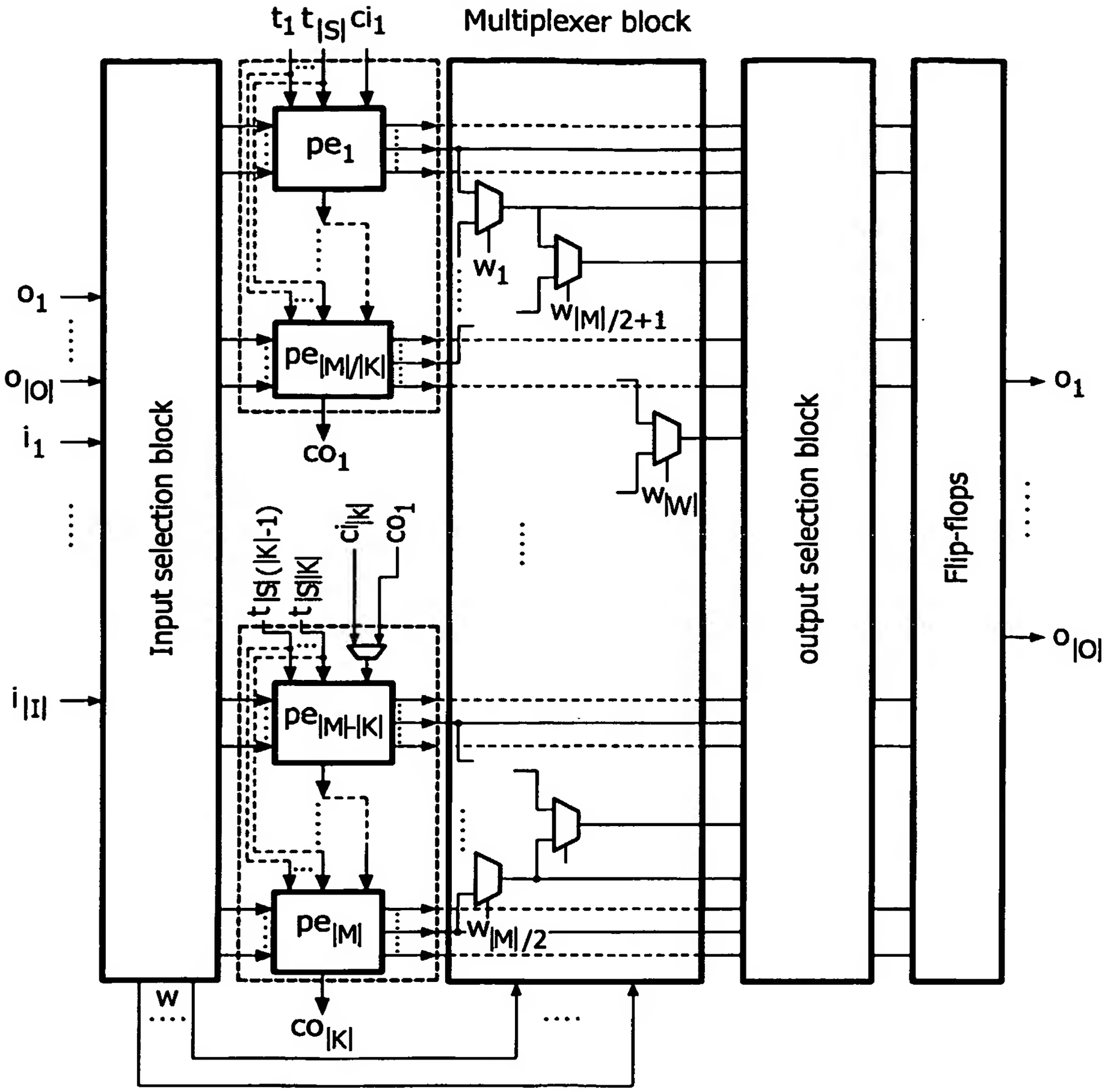
t_1 $t_{|S|}$ ci_1
Multiplexer block
pe_1
$pe_{|M|/|K|}$
$pe_{|M|-|K|}$
$pe_{|M|}$
co_1
$co_{|K|}$
w_1
$w_{|M|/2+1}$
$w_{|M|}$
$w_{|M|/2}$
o_1
$o_{|O|}$
i_1
$i_{|I|}$
Input selection block
output selection block
Flip-flops
$t_{|S|(|K|-1)}$
$t_{|S|K|}$
$ci_{|K|}$
co_1
w

FIG. 8

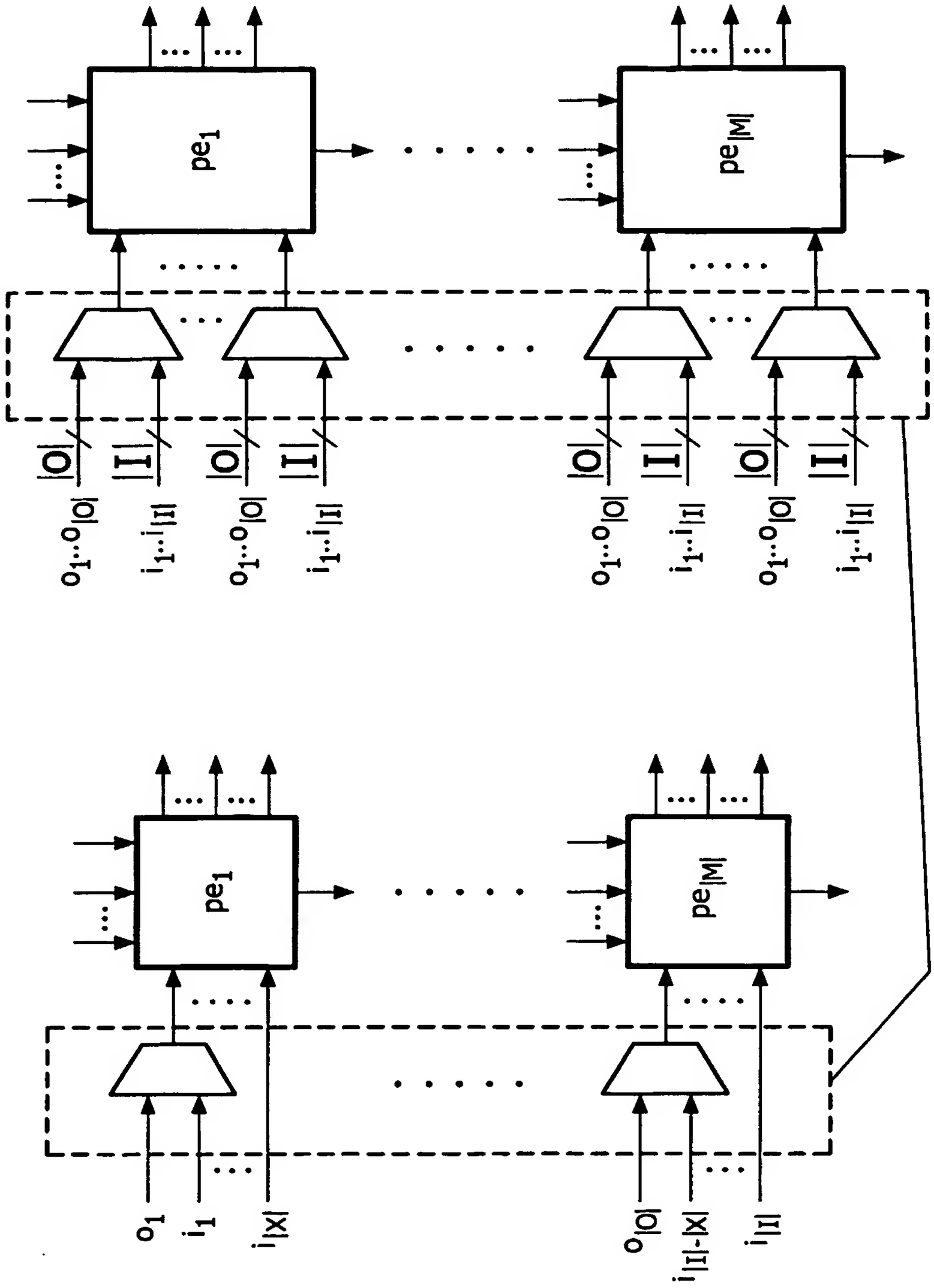

FIG. 9b

FIG. 9a

TYPE	I	O
Data-path oriented	|X|* |M|	|Y|* |M|
Random-logic oriented	max(|X|/2*(|M| +1), |X|* |M|*2)	|Y|* |M|
Memory-oriented	|X|* |M|	|Y|* |M|

FIG. 10

TYPE	Boolean	Arithmetic	Memory
Data-path oriented	log |M|* (log |N| + 2)	|M| * |N|	-
Random-logic oriented	log |M|* (log |N| + 4)	|M| * |N|	-
Memory-oriented	log |M|* (log |N| + 5)	2* |M| * |N|	2* |M| * |N|

FIG. 11

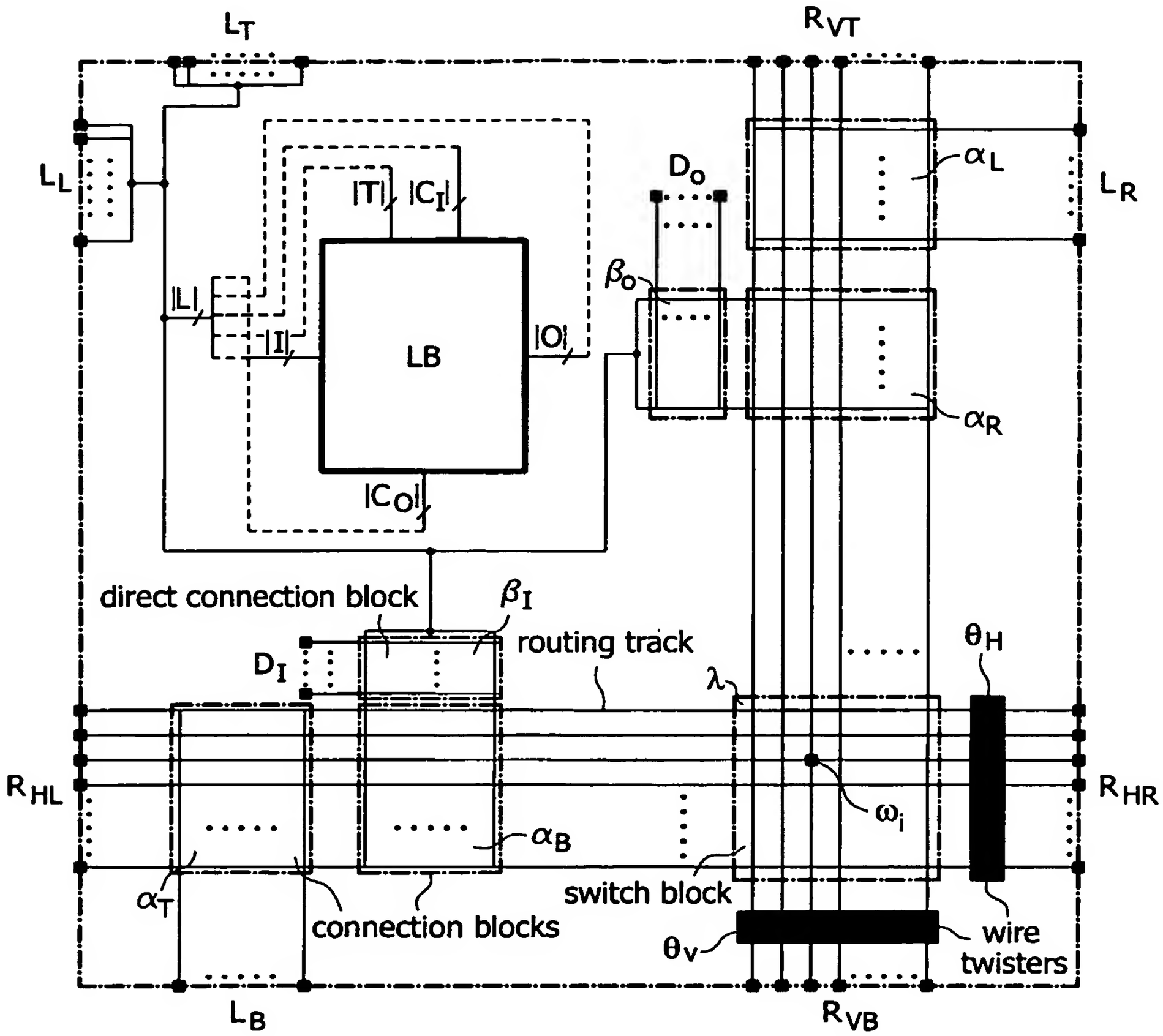
L_T
R_{VT}
L_L
|T|
$|C_I|$
|L|
|I|
LB
|O|
$|C_O|$
D_O
β_O
α_L
L_R
α_R
direct connection block
β_I
routing track
D_I
θ_H
λ
R_{HL}
R_{HR}
ω_i
α_B
α_T
switch block
connection blocks
θ_V
wire twisters
L_B
R_{VB}

FIG. 12

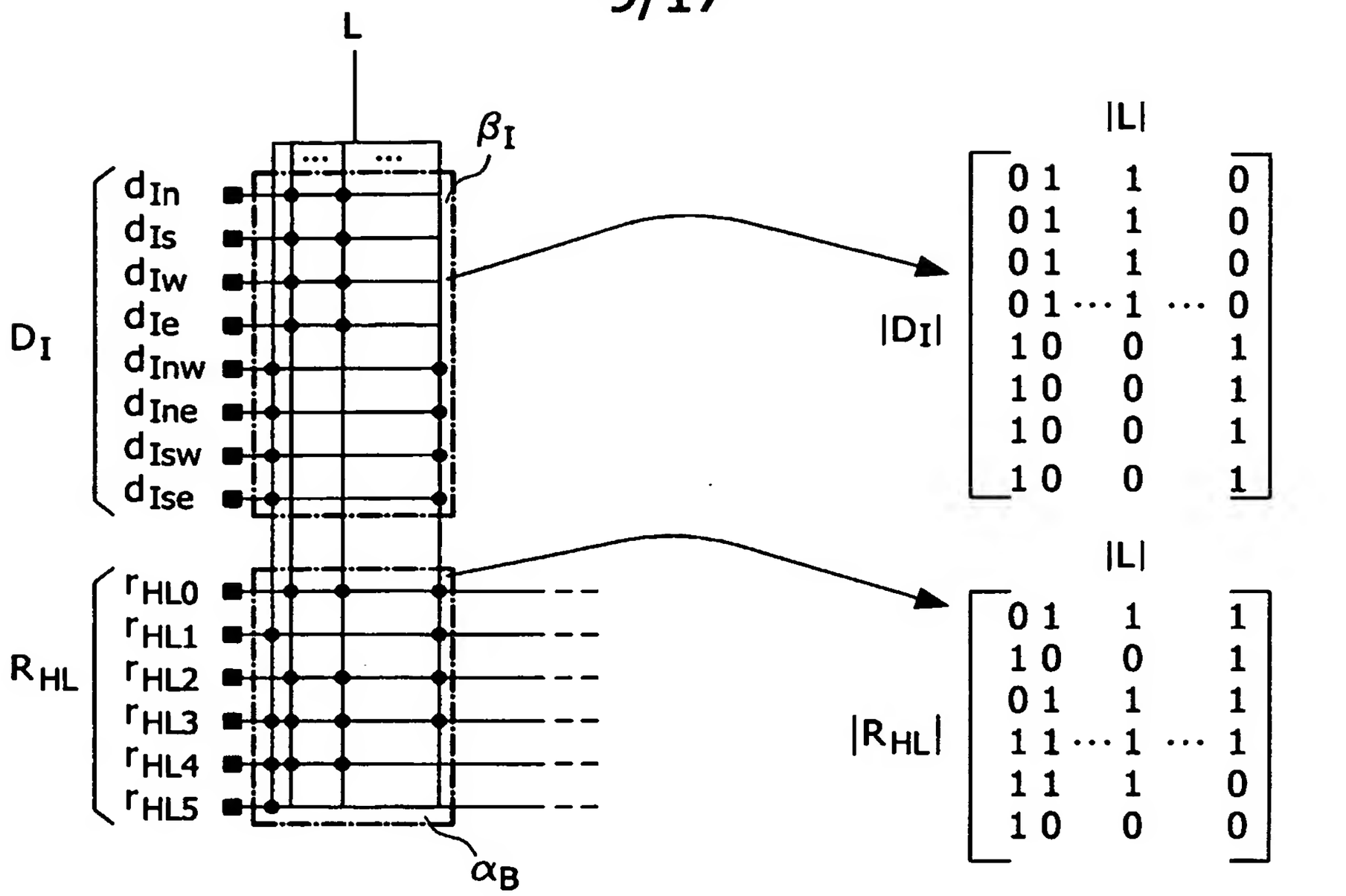

FIG. 13a

FIG. 13b

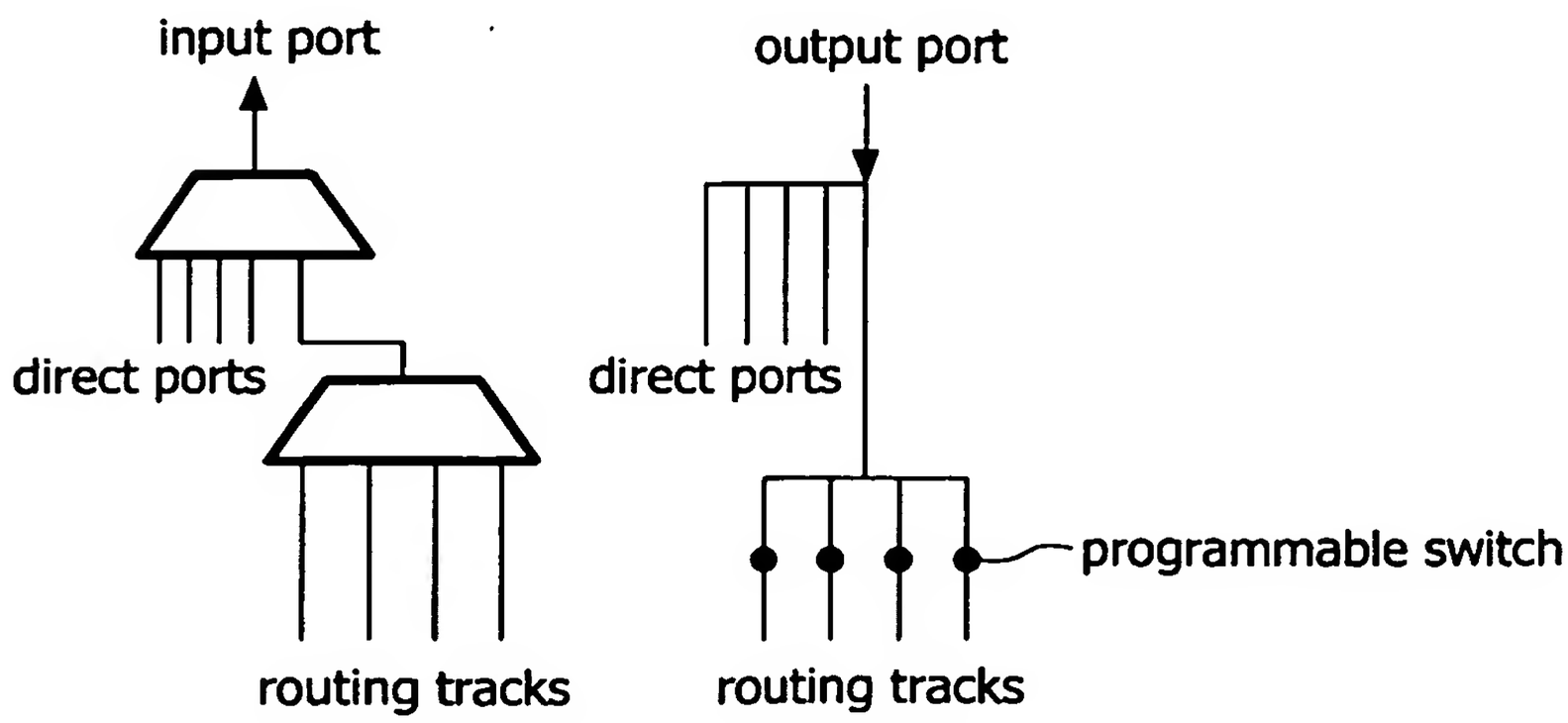

FIG. 13c

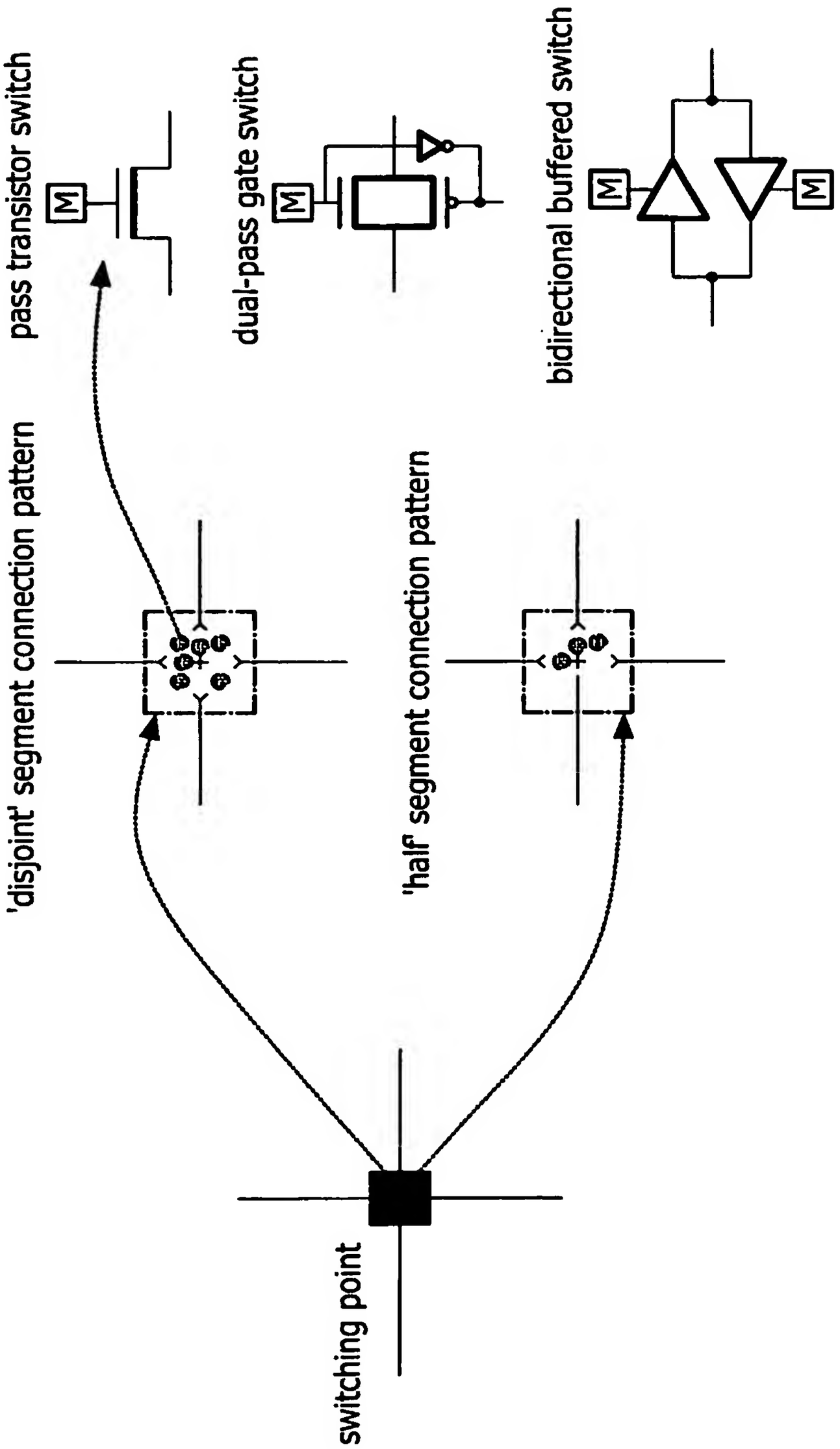

FIG. 14b

FIG. 14a

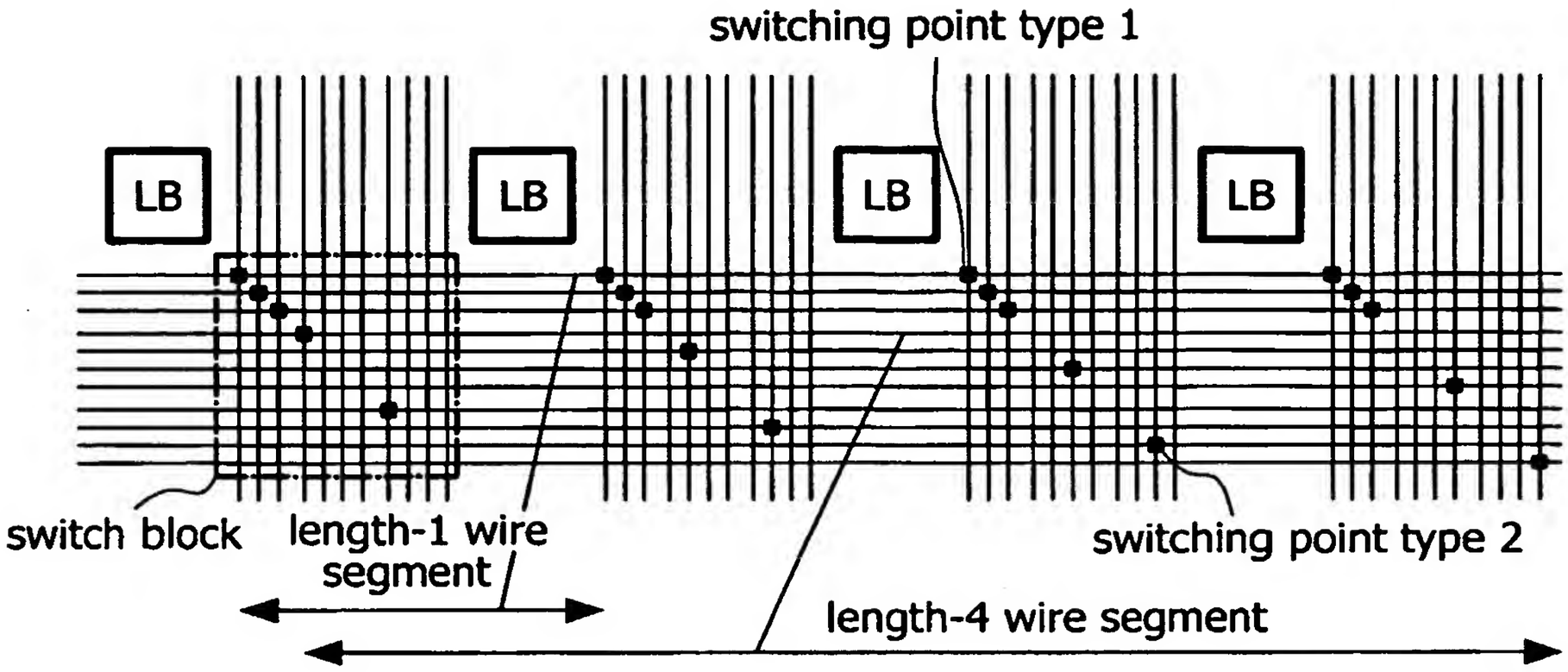

FIG. 15a

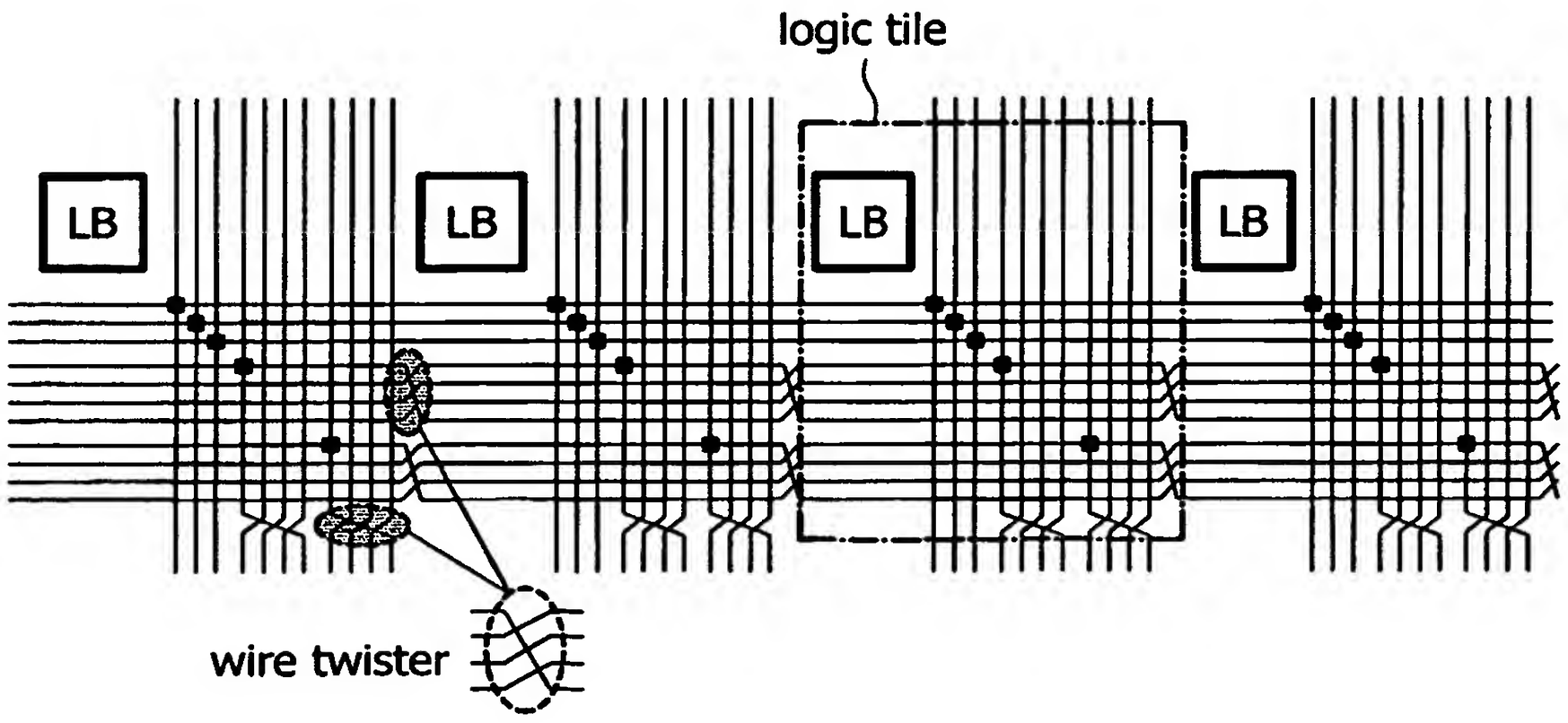

FIG. 15b

Switching matrix

$$\begin{bmatrix}
1&0&0&0&0&0&0&0&0&0\\
0&1&0&0&0&0&0&0&0&0\\
0&0&1&0&0&0&0&0&0&0\\
0&0&0&2&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&2&0&0&0\\
0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0\\
0&0&0&0&0&0&0&0&0&0
\end{bmatrix}$$

Twist matrix

$$\begin{bmatrix}
1&0&0&0&0&0&0&0&0&0\\
0&1&0&0&0&0&0&0&0&0\\
0&0&1&0&0&0&0&0&0&0\\
0&0&0&0&0&0&1&0&0&0\\
0&0&0&1&0&0&0&0&0&0\\
0&0&0&0&1&0&0&0&0&0\\
0&0&0&0&0&1&0&0&0&0\\
0&0&0&0&0&0&0&0&0&1\\
0&0&0&0&0&0&0&1&0&0\\
0&0&0&0&0&0&0&0&1&0\\
0&0&0&0&0&0&0&0&0&1&0
\end{bmatrix}$$

FIG. 15c

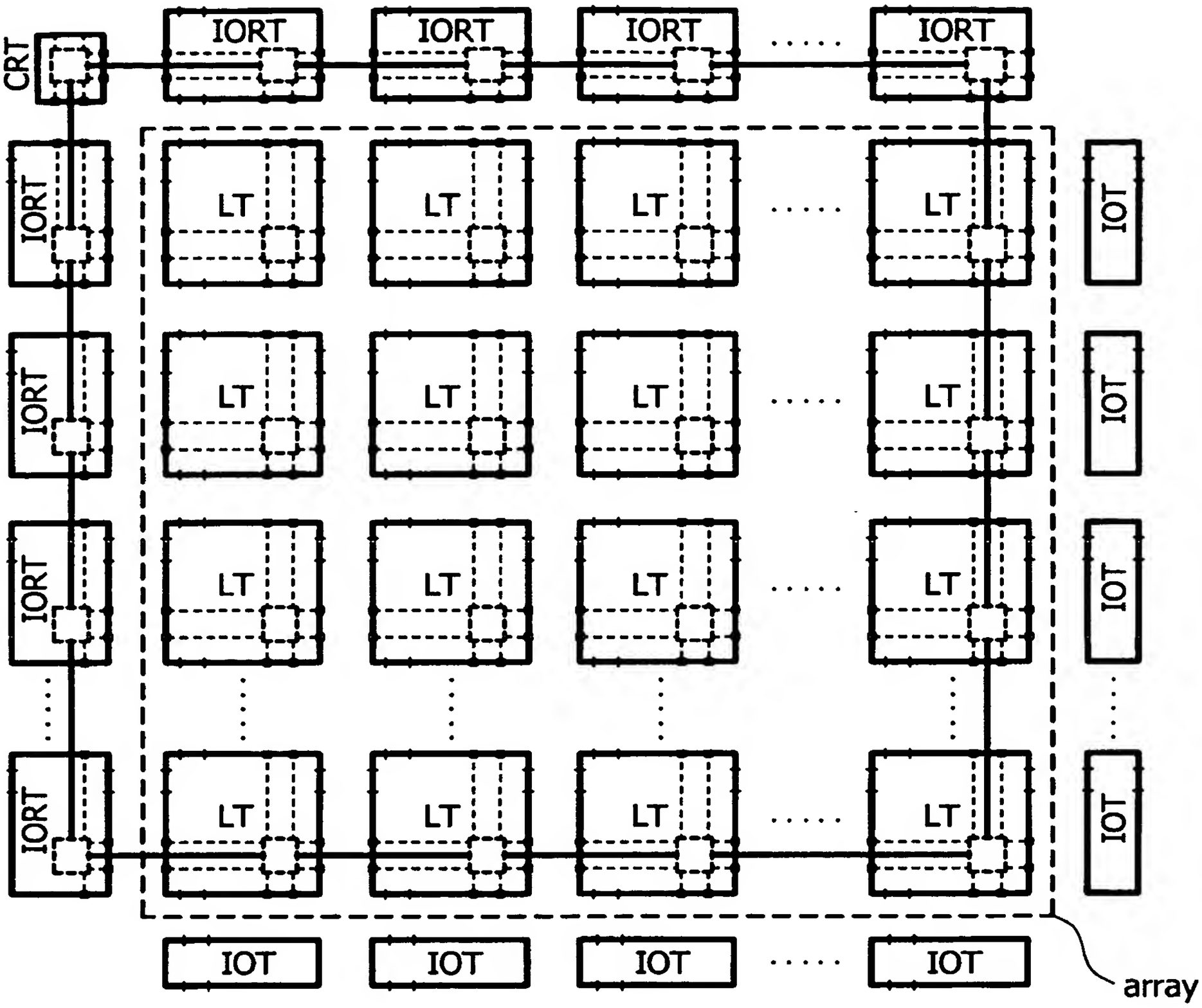

FIG. 16

Input/Output Tile with Routing (IORT): top

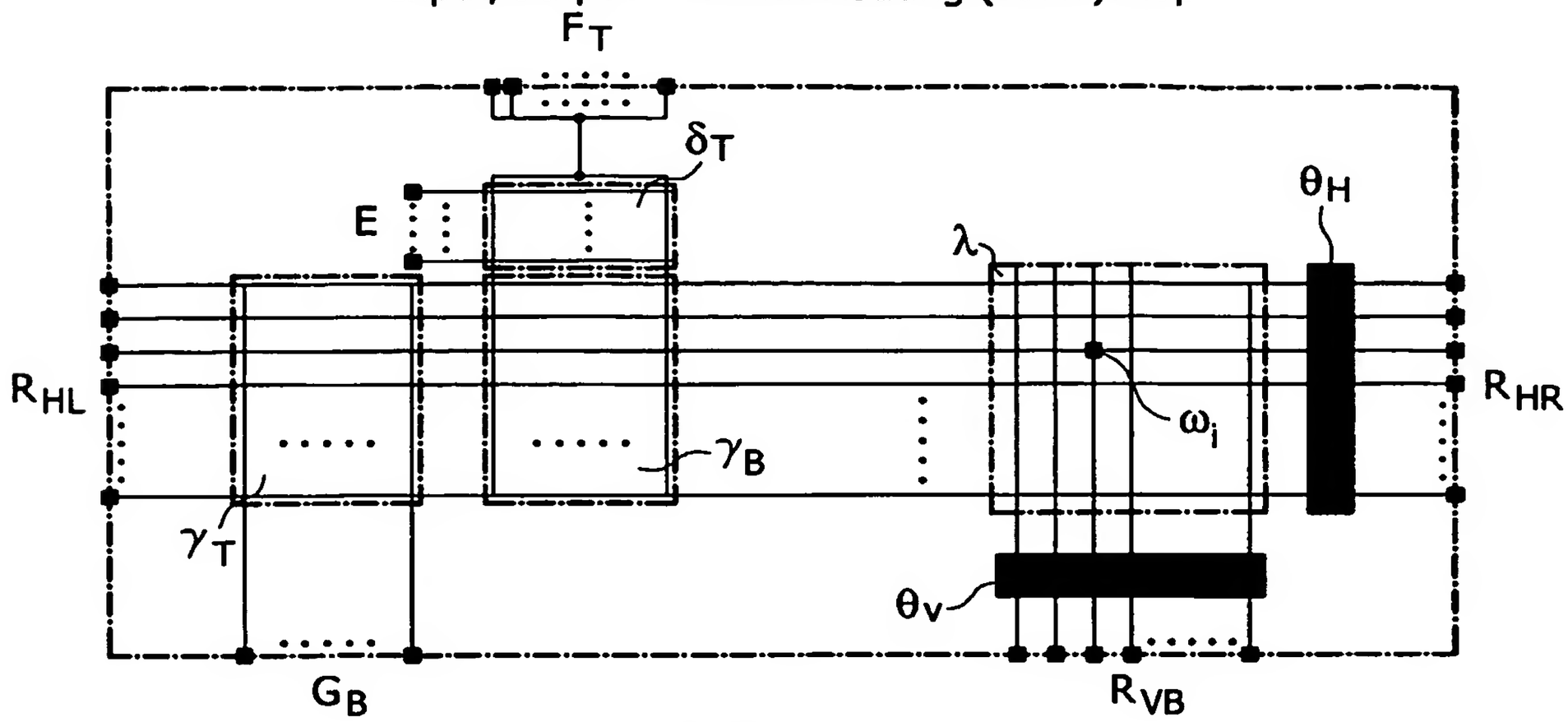

FIG. 17a

Input/Output Tile with Routing (IORT): left

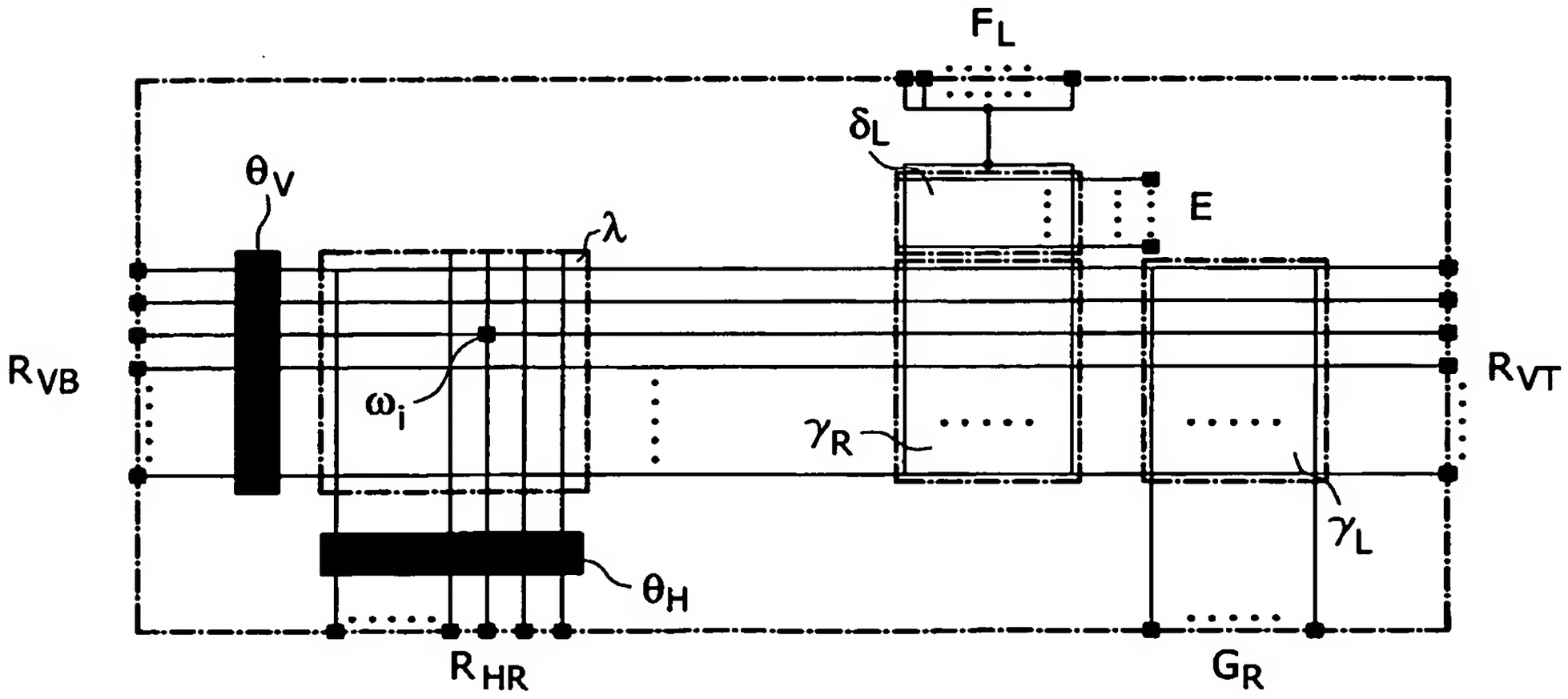

FIG. 17b

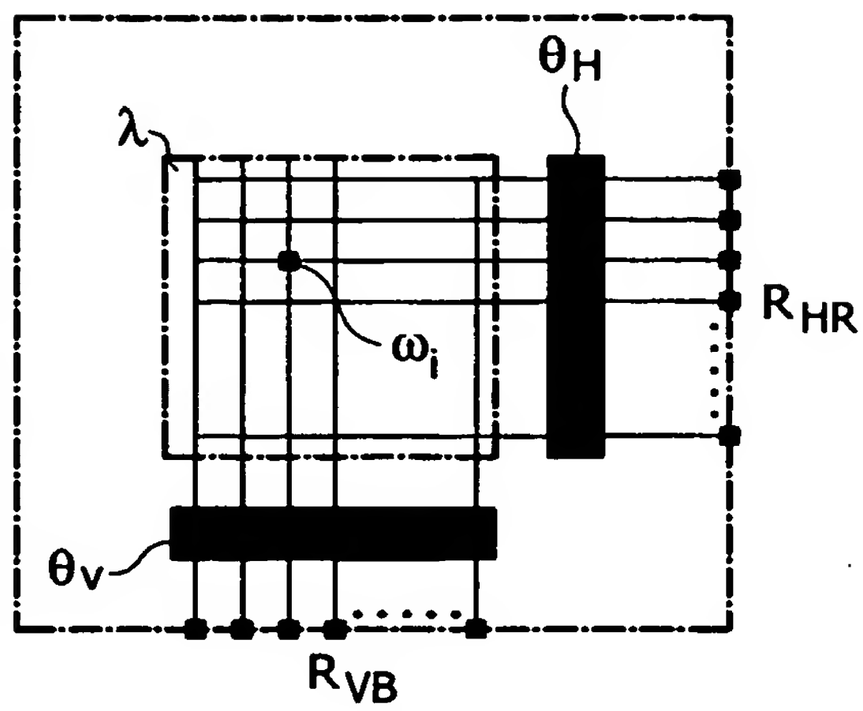
Corner Routing Tile (CRT)
θ_H
λ
ω_i
R_{HR}
θ_V
R_{VB}

FIG. 17c

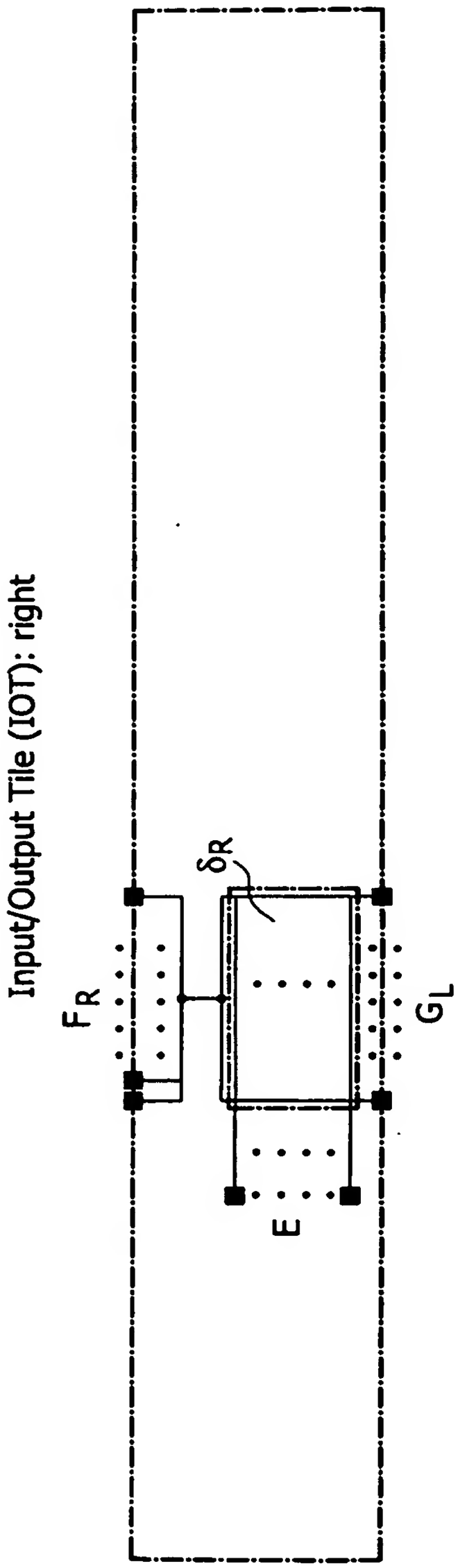

FIG. 18a

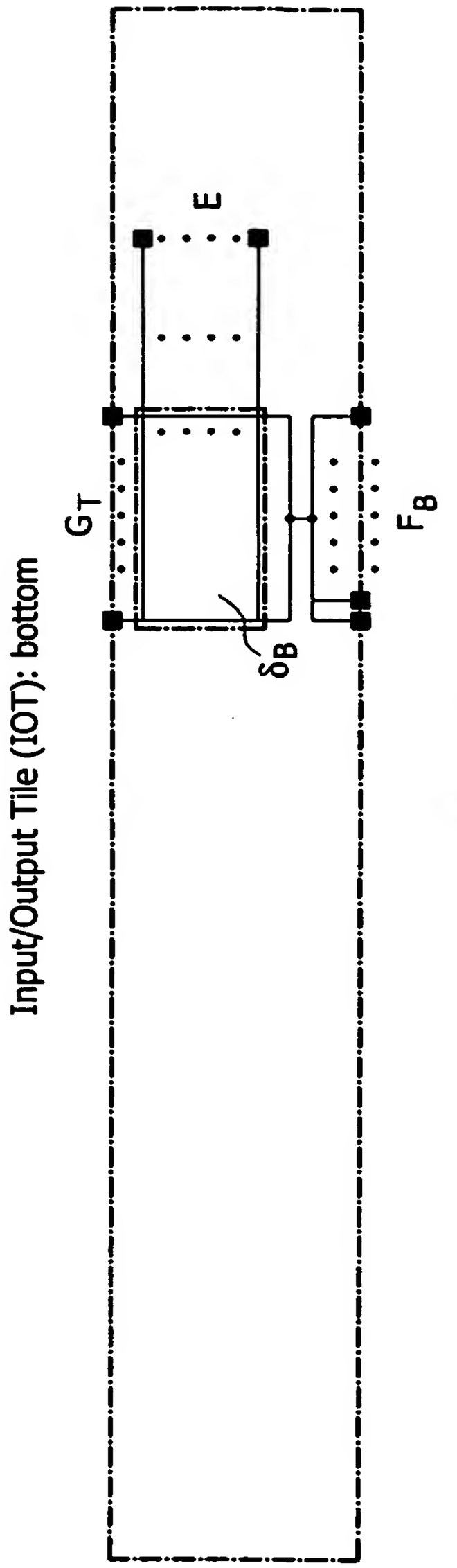

FIG. 18b

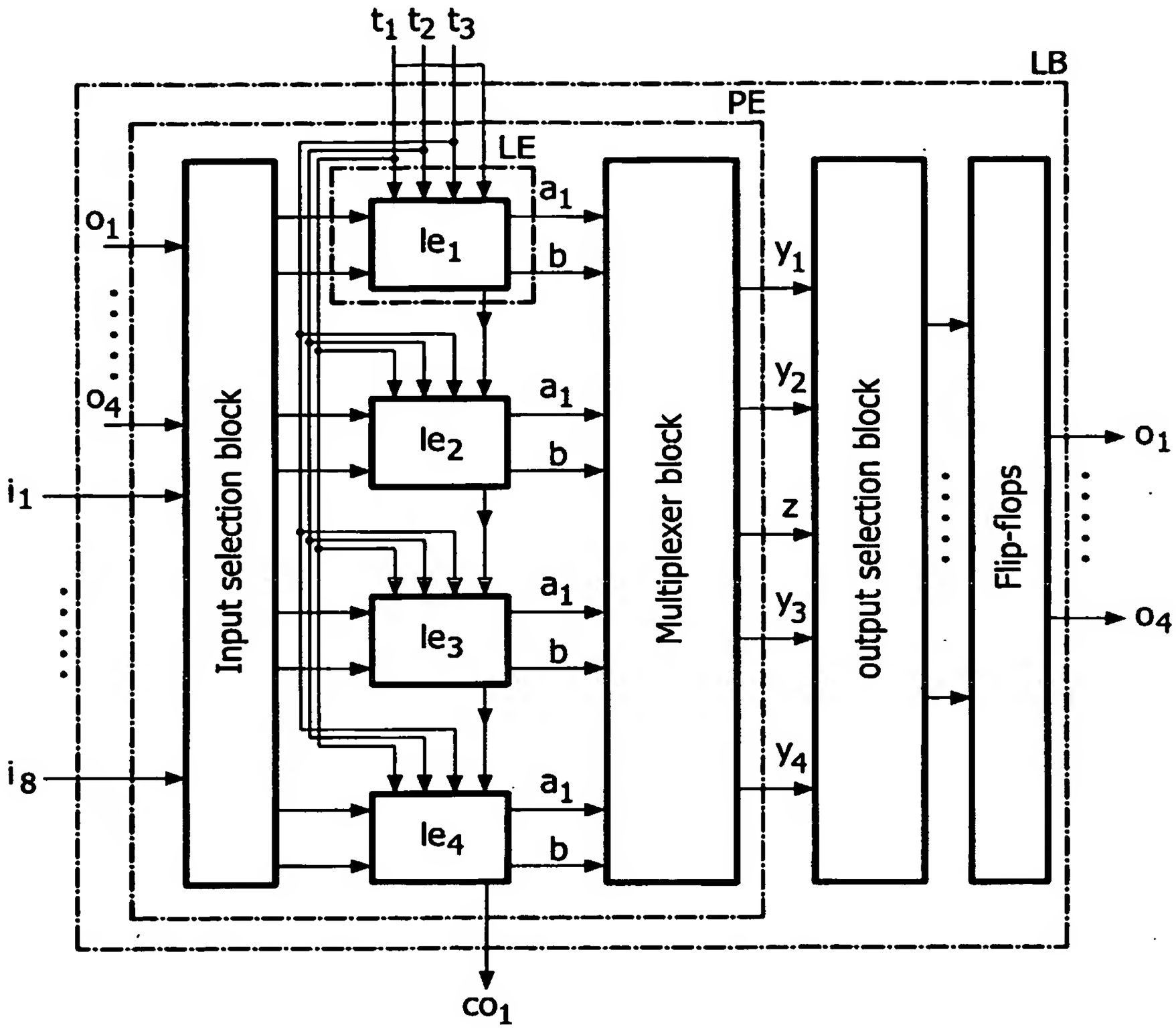
t1 t2 t3
LB
PE
LE
a1
o1
le1
b
y1
o4
le2
y2
i1
z
le3
y3
i8
le4
y4
Input selection block
Multiplexer block
output selection block
Flip-flops
o1
o4
co1

FIG. 19